INTRODUCTION

After startup, PLC checks the status of real world input devices (like switches, sensors etc.) connected to PLC input module terminals and updates the corresponding bit of Input and Output Image Status Table. PLC then executes the user program instructions using input image status table and according to program instruction results, updates the Output Image Status Table. After the end of program scan cycle, the output status table contents are transferred to real world output devices through output modules. The output devices may be a lamp, a relay coil, a motor startor etc.

In this chapter, we will discuss basics of ladder diagram and its instructions.

3.1 LADDER DIAGRAM

Ladder logic diagrams are normally used in PLC to write program instructions. **Ladder logic language** uses input and output symbols and is a graphic based language. **The ladder diagram represents program steps using inputs and outputs symbols like in a electrical relay diagram.** A sample ladder diagram is shown in fig. 3.1.

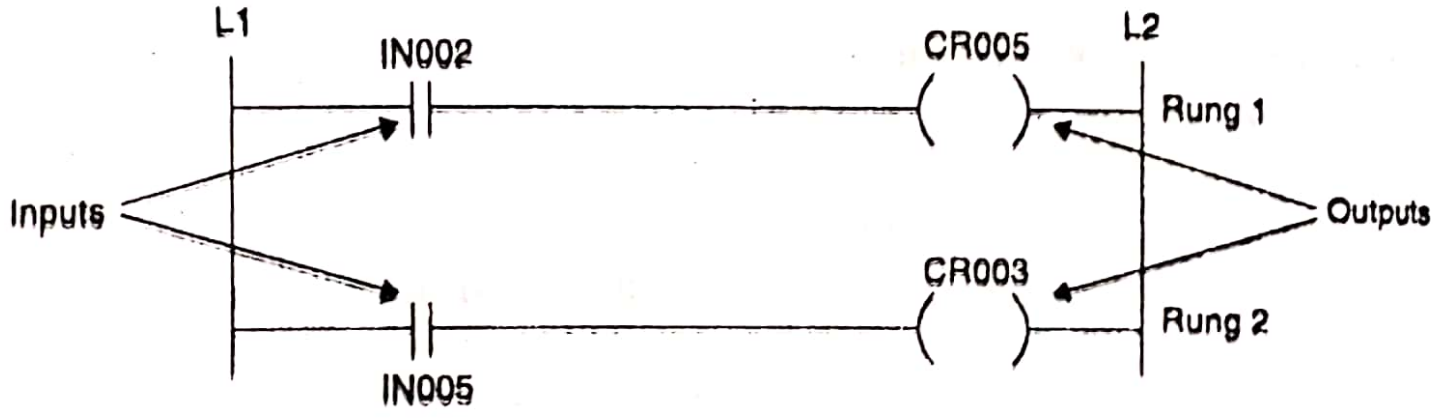


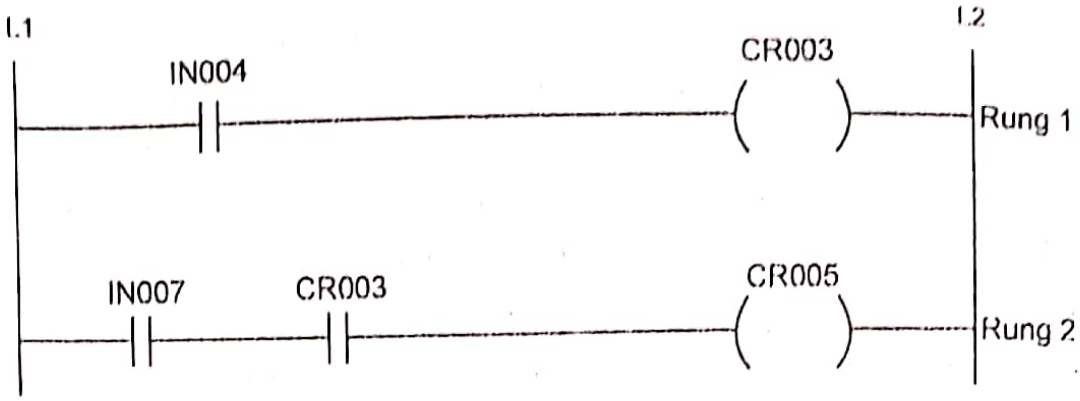
Fig. 3.1 : Ladder Diagram

The two vertical lines L1 and L2 are called **Rails.** These rails represents the two supply lines (Phase and Neutral for AC supply system. Positive and Negative for DC supply system) for the ladder diagram. One horizontal row of elements between the rails of a ladder program is called a **Rung.** A rung contains input and output elements. There can be one or more than one input elements in a rung and are represented on the left side of the rung. Output is represented on the right side of the rung. The inputs and outputs are called by different names and addressed using different notations by different manufacturers. For example, inputs are called inputs, contacts, words, functions and instructions (like Examine ON and Examine OFF) etc. **Discrete Inputs are addressed** as IN 001, IN007 or I : 2/0, I : 5/4 etc. depending upon the PLC manufacturer. Normally all manufacturers Input/Output addressing technique uses alphabets to represent type of Input/Output and the number to represent the I/O module and terminal number. In the same way, outputs are called, outputs, coils, instruction etc. **Discrete Outputs are addressed as CR003, CR015 etc. or as O : 7/3, O : 1/6 etc.** In this book, both type of I/O addressing is used.

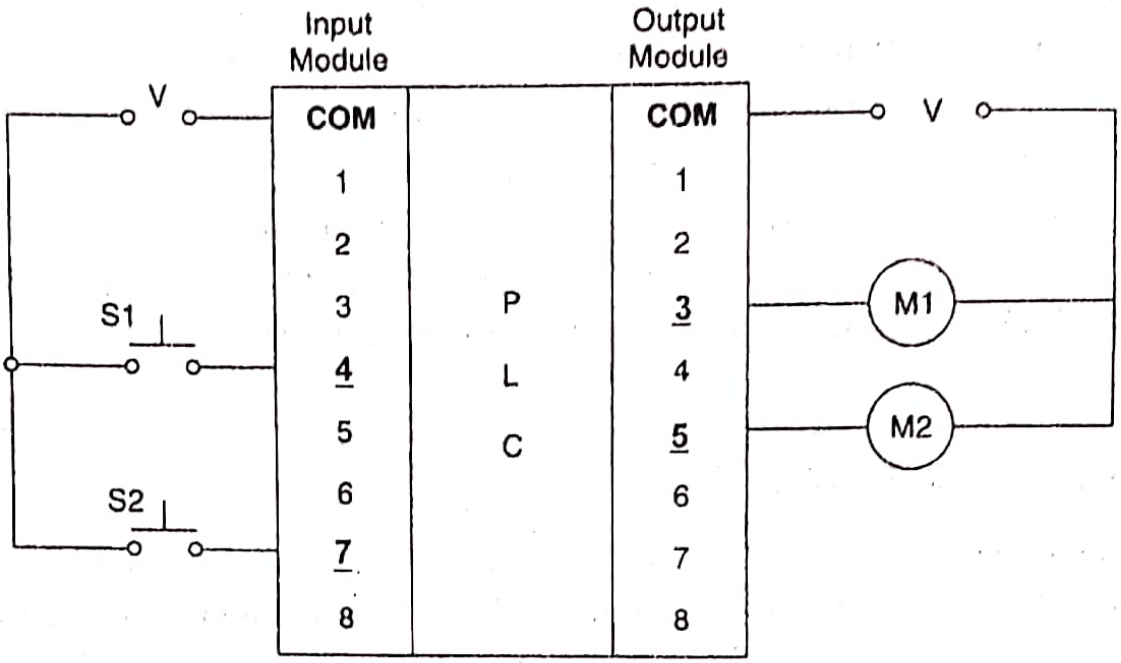
3.2 LADDER PROGRAM EXECUTION

A ladder program may have one or more rungs and is executed from Left to Right and Top to Bottom. After the input scan, the controller looks at the inputs of first rung. This logic problem is solved based on the state of elements stored in the PLC memory. This includes all inputs according to the input image status table contents, and all internal status bits, latches or outputs according to their last known state. After the input logic has been solved, the output is energised/ de-energised (corresponding memory bit is set/reset) depending upon the solution is True/False. Once this is done, the controller moves to the next rung of the logic and repeats the procedure. Once output of a rung is set or reset, it remains in that state untill the rung is again solved in the next program scan. If an input associated with an output is used in later rungs, the condition of the input (True or False) will be based on the status of output at the time of its input usage. After the last rung of the program is solved, the contents of output image status table are transferred to output devices through output terminals of the output modules.

Figure 3.2 shows Ladder diagram and connection diagram of a simple program.



(a) Ladder Diagram



(b) Connection Diagram

Fig. 3.2 : Ladder adder and Connection Diagram

During the input scan (also called input update) status of switches S1 (IN004) and S2 (IN007) are read and stored in input image table. Say at that time S1 is ON and S2 is OFF. During program scan, first rung 1 is solved. In this case, since IN004 (S1) is True, the memory bit in Output image table corresponding to CR003 output is set (high). Then rung 2 is solved. In this rung, inputs IN007 (S2) and CR003 contact are connected in AND logic *i.e.* when both inputs are true then only output will be set otherwise output is reset. In present case IN007 is false while contact CR003 is true (from the result of Scan1) and thus input logic of rung 2 is false. So the memory bit in output image table corresponding to CR005 output is reset (low). Then during output scan (also called output update), the status of output image table is transferred to output module *i.e.* output M1 (CR003) is turned ON and output M2 (CR005) is turned OFF. After output scan, input scan starts and whole process is repeated. It is important to note that, input contact CR003 does not exist physically but is implemented logically. It goes ON and OFF with output coil CR0003.

3.3 BASIC INSTRUCTIONS

Different PLC manufacturers may have different mnemonics and addressing styles for writing ladder programs. But, once the basics of PLC operation and programming in ladder logic is clear, adapting to the various manufacturers devices is not a complicated process. In this book, we will discuss the instructions mnemonics used by **Allen-Bradley** PLCs.

Basic instructions when used in ladder programs, represents hardwired logic circuits used for the control of a machine or equipment. These basic instructions are separated into three groups :

- Bit Instructions
- Timer Instructions
- Counter Instructions.

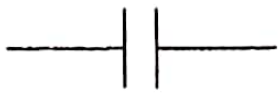
Table 3.1 : Shows bit instructions

Mnemonic	Name	Instruction Type	Purpose
XIC	Examine If Closed	Input	Examines a bit for ON condition
XIO	Examine If Open	Input	Examines a bit for OFF condition
OTE	Output Energize	Output	Turns a bit ON or OFF
OTL	Output Latch	Output	Turns a bit ON when the rung is executed and this bit retains its state when the rung is not executed or a power cycle occurs.
OTU	Output Unlatch	Output	Turns a bit OFF when the rung is executed and this bit retains its state when the rung is not executed or a power cycle occurs
OSR	One-shot Rising	Input	Triggers a one-time event

Table 3.1 : Bit instructions

3.4 EXAMINE IF CLOSED (XIC)

XIC instruction (normally open contact input) is used to determine if a bit is ON. When the instruction is executed, if the addressed bit is ON (1), then the instruction is evaluated as True, and if OFF (0) then evaluated as FALSE



(a) XIC Instruction Symbol

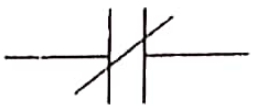
Addressed Bit State	XIC Instruction Result
OFF (0)	False
ON (1)	True

(b) Logic Table for XIC

Fig. 3.3 : XIC Instruction

3.5 EXAMINE IF OPEN (XIO)

XIO instruction (normally closed contact input) is used to determine if a bit is off. When the instruction is executed, if the addressed bit is OFF (0) then the instruction is evaluated as TRUE and if ON (1) then evaluated as FALSE.



(a) XIO Instruction Symbol

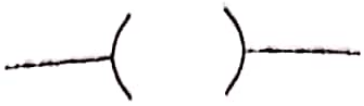
Addressed Bit State	XIO Instruction Result
OFF (0)	True
ON (1)	False

(b) Logic Table for XIO

Fig. 3.4 : XIO Instruction

3.6 OUTPUT ENERGIZE (OTE)

OTE instruction (coil output) is used to control an output bit state. When the instruction is executed, if the rung condition is TRUE then the addressed output bit is set to 1 (energised) and if FALSE then reset to 0 (de-energised).



(a) OTE Instruction Symbol

Rung Condition	Addressed Output Bit
True	1 (Energised)
False	0 (De-energised)

(b) Logic Table of OTE

Fig. 3.5 : OTE Instruction

The output bit remains set or reset (energised or de-energised) for one scan-cycle i.e. till the same instruction is executed again in the next scan cycle.

3.7 LADDER DIAGRAM FOR BOOLEAN LOGIC OF INPUTS

In process control applications, output condition may depends upon logical combination (AND, OR, XOR etc.) of inputs. These logical combinations can be easily made in ladder diagram.

3.7.1 AND Combinations

For logical 'AND' combinations of two or more inputs, the inputs are put in series. The rung condition will be TRUE only if all the inputs are TRUE (1). If even a single input is FALSE (0) then the rung condition will be FALSE.

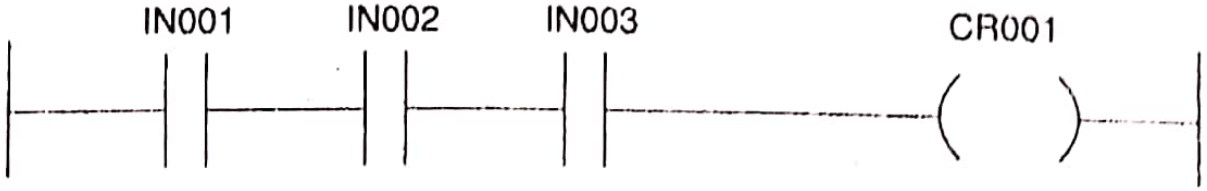


Fig. 3.6 : AND Combination of Inputs

3.7.2 OR Combinations

For logical 'OR' combination of two or more inputs, the inputs are put in parallel to each other. The rung condition will be TRUE if any of the inputs is TRUE (1). If all the inputs are FALSE (0), then only the rung condition will be FALSE.

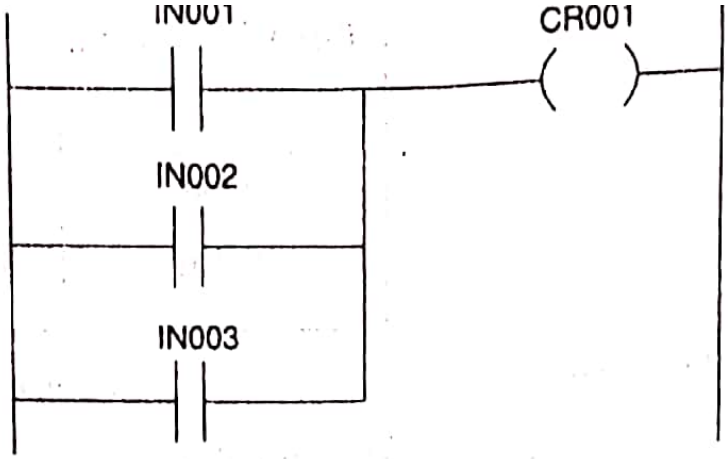
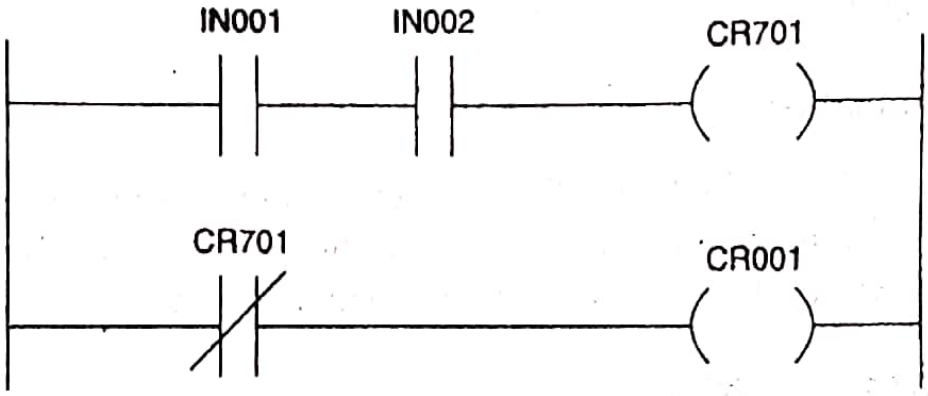


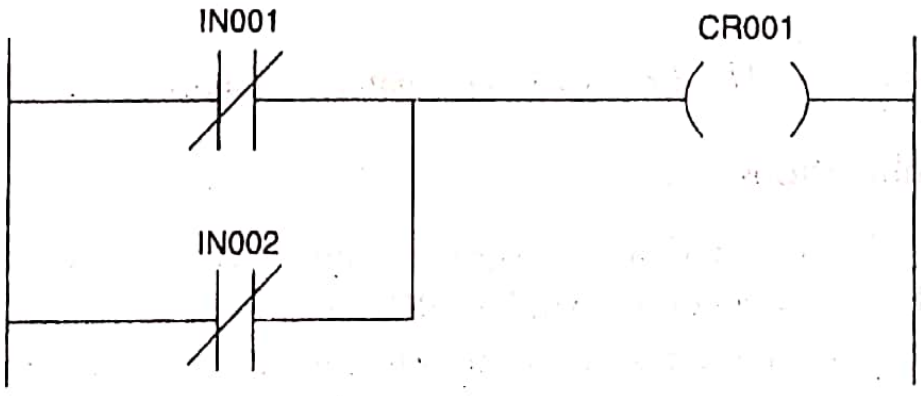
Fig. 3.7 : OR Combination of Inputs

3.7.3 NAND Combination

Figure 3.8 shows NAND combination of two inputs in two different ways. The rung condition will be FALSE only if all the Inputs are TRUE (1). If any input is FALSE (0), then rung condition will be TRUE.



(a) NAND Combination using Internal Latch



(a) NAND Combination without using internal Latch

Fig. 3.8 : NAND Combination of Inputs

3.7.4 NOR Combination

For 'NOR' combination, normally closed contacts of inputs are put in series. The rung condition will be TRUE only if all the inputs are FALSE (0). If any of input is TRUE (1), then the rung condition will be FALSE.

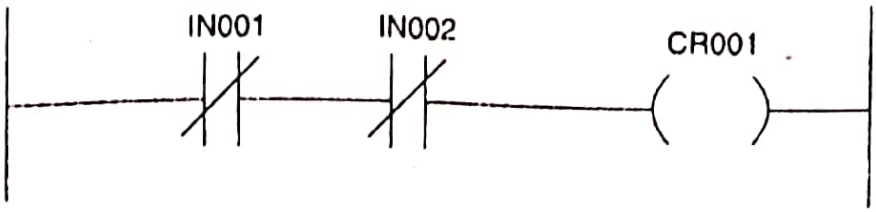


Fig. 3.9 : NOR Combination of Inputs

3.7.5 XOR Combination

Figure 3.10 shows XOR combination for two inputs. The rung condition will be FALSE if both the inputs are either FALSE (0) or TRUE (1). If one input is TRUE (1) and other is FALSE (0), then the rung condition will be TRUE.

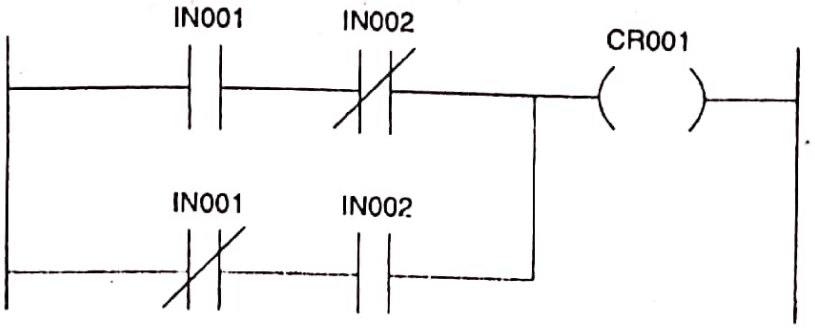


Fig. 3.10 : NOR Combination of Inputs

3.7.6 XNOR Combination

Figure 3.11 shows XNOR combination for two inputs. The rung condition will be TRUE if both the inputs are either FALSE (0) or TRUE (1) If one input is TRUE (1) and other is FALSE (0), then the rung condition will be FALSE.

XNOR of A, B = $(A + \overline{B}) . (\overline{A} + B)$